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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/842,100	04/25/2001	Douglas Sojourner	10991096-1	6956	
759	90 10/10/2002				
AGILENT TECHNOLOGIES Legal Department, 51U-PD Intellectual Property Administration P.O. Box 58043 Santa Clara, CA 95052-8043			EXAM	EXAMINER	
			DI GRAZIO,	DI GRAZIO, JEANNE A	
			ART UNIT	PAPER NUMBER	
			2871		
			DATE MAILED: 10/10/2002	!	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)			
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Office Astice Occurrence	09/842,100	SOJOURNER ET AL.			
Office Action Summary	Examiner	Art Unit			
The MAN INC DATE And	Jeanne A. Di Grazio	2871			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status					
1) Responsive to communication(s) filed on					
<u> </u>	– · s action is non-final.				
3) Since this application is in condition for allowar		osecution as to the merits is			
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims					
4) Claim(s) 1-18 is/are pending in the application.					
4a) Of the above claim(s) is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.					
6)⊠ Claim(s) <u>1-18</u> is/are rejected.					
7) Claim(s) is/are objected to.					
8) Claim(s) are subject to restriction and/or election requirement. Application Papers					
9) The specification is objected to by the Examiner.					
10)⊠ The drawing(s) filed on <u>25 April 2001</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.					
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
11) The proposed drawing correction filed on	is: a) ☐ approved b) ☐ disappro	ved by the Examiner.			
If approved, corrected drawings are required in reply to this Office action.					
12)☐ The oath or declaration is objected to by the Examiner.					
Priority under 35 U.S.C. §§ 119 and 120					
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).					
a) All b) Some * c) None of:					
1. Certified copies of the priority documents have been received.					
2. Certified copies of the priority documents have been received in Application No					
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 					
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).					
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.					
Attachment(s)					
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal P	(PTO-413) Paper No(s) Patent Application (PTO-152)			



Art Unit: 2871

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DETAILED ACTION

Specification

Please note that on page 4 line 9 of the specification, the sentence should read: "FIG.1 depicts an example of a top view of a prior art lcmd substrate assembly."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar (USPN 6,177,288 B1) in view of Kitamura (JP09066429).

Per method claims 1-8: Creating a hole in a substrate; causing liquid crystal to flow through said hole; and sealing said hole.

- Testing said lcmd after sealing said hole.
- Separating said lcmd from other lcmds after testing said lcmd.
- The substrate is a semiconductor substrate.
 - o The semiconductor substrate comprises:
 - an integrated circuit.
 - is part of a silicon wafer.
- The substrate comprises glass.
- The hole is sealed using a sealant material selected from a group consisting of glue, epoxy, and solder.

Discussion (per claims 1-8): Takiar does not disclose a method of manufacturing a liquid crystal micro display; however, Takiar does disclose a method of manufacturing a chip scale integrated circuit package and testing method for such package. Kitamura, furthermore, discloses that a liquid crystal can be injected directly into an injection hole



Application/Control Number: 09/842,100

Art Unit: 2871

of a liquid crystal substrate. It would have been obvious at the time the invention was made, to one of ordinary skill in the art, to combine the technology of Kitamura with that of Takiar to a method of manufacturing a liquid crystal micro display that contains an integrated circuit and semiconductor device because a liquid crystal micro display with an IC and semiconductor circuit is clearly within the scope of Takiar's invention.

Takiar discloses that the chip scale packages are individually electrically tested while remaining physically connected to one another and then after individual testing, the chip scale packages are then separated from each other [Col. 2, Lines 41-45]. It would have been obvious at the time the invention was made, to one of ordinary skill in the art of liquid crystal micro displays, to test after sealing the liquid crystal and then to separate the individual micro displays because the method of applying an encapsulating material over the top of the substrate (as disclosed in Takiar, Col. 2, Lines 57-60) to form the plurality of chip scale packages (Id.) is analogous to sealing a liquid crystal prior to testing.

Semiconductor substrates, glass substrates, integrated circuits, and silicon wafers are all common in the art of liquid crystal and semiconductor manufacturing.

A sealant material of glue, epoxy, and solder are common in the art of liquid crystal and semiconductor technology.

Per method claims 9-13: Testing said first lcmd while it is physically connected to a second lcmd; and separating said first lcmd from said second lcmd.

- The first lcmd:
 - o comprises a semiconductor substrate having an integrated circuit and a glass substrate having a transparent electrode
- The integrated circuit comprises electrodes.
- The testing includes:
 - o causing a voltage difference between the integrated circuit electrodes and the transparent electrode.
 - o determining whether the lcmd produces a uniform image.

Application/Control Number: 09/842,100

Art Unit: 2871

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Discussion: Takiar discloses testing individual chip scale packages prior to their separation form each other. Takiar discloses an IC circuit. An IC circuit will comprise electrodes. Glass substrates comprising electrodes are common in the art of liquid crystal technology. Takiar discloses electrically testing each individual chip scale package. It would have been obvious at the time the invention was made, to one of ordinary skill in the art, to determine whether an lcmd produces a uniform image because uniformity of image is paramount to liquid crystal displays.

Per apparatus claims 14-18: A first substrate and a second substrate having a hole extending through a thickness thereof.

- The hole can be used for filling the lcmd with liquid crystal material.
- The second substrate:
 - o is a semiconductor substrate comprising an integrated circuit.
 - o comprises glass.
- The lcmd is physically connected to other lcmds.

Discussion: Kitamura discloses that a liquid crystal material can be injected through an injection hole of the liquid crystal substrate. Semiconductor substrates with IC circuits and glass substrates are common in the art of liquid crystal technology. Takiar discloses chip scale integrated circuits physically connected to each other as noted and discussed previously.

Application/Control Number: 09/842,100

Art Unit: 2871

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (703)305-7009. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Sikes can be reached on (703)308-4842. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-8741 for regular communications and (703)746-8741 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jeanne Andrea Di Grazio

ames A. Dudek, Primary Examiner

JDG

October 2, 2002